Amendments to the Specification:

Please amend the specification as follows:

[20]   FIG. 4 is a functional block diagram of a test system 400 including a test management unit (TMU) 21, which may be formed from a Field Programmable Gate Array (FPGA), and which operates as a test pattern decoder to interface multiple chip pins 23 of a DUT 1 to a single test channel 27 of a tester 20 according to one embodiment of the present invention. Only one test channel 27 of the tester 20 is shown in Fig. 4, although the tester includes a number of such test channels coupled to the TMU 21. A compression-decompression scheme as previously discussed can be implemented on the TMU 21 such that the test channel 27 can input a relatively small number of bits and then the TMU can decompress the small number into a larger number of bits for input to multiple scan chains (not shown in Fig. 4) within the DUT 1. Specifically, m bits of an output-disabled-encoded-I/O signal EN-I/O* are fed to the TMU 21. The TMU 21 decodes the output-disabled-encoded-I/O signal EN-I/O* into n bits of an output-disabled-decoded-I/O signal DE-I/O*. Here, m<n<2**m +1. The n bits of the output-disabled-decoded-I/O signal DE-I/O* are then fed into respective scan chains within the DUT 1. In this way, each scan chain has its own unique pattern of input data defined by the corresponding bits of the DE I/O* signal.

—nth bit

Entry not approved. 1/22/2007 TR

[23]   In operation, the tester 20 initially applies the OFR-In signals to the DUT 1 to initialize the contents of the OFR 22, and also applies the EN-I/O* signals to the TMU 21 which, in turn, decodes these signals to develop the DE-I/O* signals that are applied the pins 23 of the DUT 1. During testing, the tester 20 applies required test data, address and control signals to the DUT 1 to control the device as required, as will be appreciated by those skilled in the art. The tester 20 thereafter receives the OFR-Out signals from the DUT 1 and determines whether these signals indicate the DUT 1 is operating properly. Note that the OFR-Out signals of Fig. 4 are intended to indicate generally output from the DUT 1 to the tester 20 during testing, and are not limited to a signature being output from the OFR 22. For example, in functional testing of the DUT 1 the OFR 22 may not be used and in this situation the OFR-Out signals correspond to test data being supplied from the DUT 1 to the tester 20 for analysis to determine whether the DUT is operating properly.

Entry is approved. 1/22/2007 TR

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